Notice of Allowability	Application No.	Applicant(s)	
	10/759,101	SHIRAMIZU ET AL.	
	Examiner	Art Unit	
	Dalzid Singh	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *20 January 2004*.

2. ☒ The allowed claim(s) is/are *1-19 which have been renumbered as 1,12,2,13,7,3,16,14,10,5,8,18,15,4,11,6,9,17 and 19 respectively*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Dalzid Singh
11/24/06

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-19 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Claim 1 is allowable because the prior art of record US Pub. No. 2004/0228636 to Pathak et al does not disclose to suggest a receiver circuit, comprising:

a synchronous circuit that recovers and outputs a clock signal having a frequency of f1/n Hz (n:2 or larger natural number) synchronized with input one data signal the data rate of which is f1 b/s (f1: positive real number);

"j" pieces of multipliers that output each clock signal acquired by multiplying a clock signal output from the synchronous circuit by predetermined multiple ratio via "j" pieces of interconnects (j: one or larger natural number); and

a synchronous digital circuit that has "j" pieces of parallel input terminals including one common to the input of the synchronous circuit, "j x k" pieces of parallel output terminals and "j" pieces of parallel clock input terminals, decides and recovers "j" pieces of data signals the data rate of each of which is f1 b/s and which are input to the "j" pieces of parallel input terminals using the "j" pieces of multiplied clock signals applied to the "j" pieces of parallel clock input terminals via (j+1) th to (2xj) th interconnects as a criterion of timing, demultiplexes the data in the ratio of "1:k" and converts to "j x k" pieces of data signals the data rate of each of which is f1/k b/s, wherein:

the "j" pieces of parallel terminals to which data signals are input of the synchronous digital circuit function as the input terminal of the receiver circuit and the "j x k" pieces of parallel terminals from which the data signals are output function as the output terminal of the receiver circuit; and

first to "j"th interconnects connecting the output terminal of the synchronous circuit and the input terminals of the "j" pieces of multipliers and "j+1"th to "2 x j"th interconnects connecting the "j" pieces of multipliers and the "j" pieces of parallel clock input terminals of the digital circuit are arranged so that delays t2max are smaller out of the maximum value t1max s of delays caused on the first to the "j"th interconnects and the maximum value t2max s of delays caused on the "j+1"th to the "2 x j"th interconnects and the delays t2max are equivalent to 1/10 or less of a clock cycle 1/f1 s output from each multiplier.

Claim 2 is allowable because the prior art of record US Pub. No. 2004/0228636 to Pathak et al does not disclose to suggest a transmitter circuit, comprising:

a synchronous circuit to which a clock signal having a frequency of f1/m/n Hz (f1: positive real number, m: one or larger natural number, n: 2 or larger natural number) is input and from which a clock signal having a frequency of f1/n Hz and synchronized with the input clock signal is output;

"j" pieces of multipliers to which the clock signals output from the synchronous circuit are input via first to "j "th (j: one or larger natural number) interconnects and

from each of which a clock signal multiplied by predetermined multiple ratio is output; and

a synchronous digital circuit that has input terminals for receiving "j x k" pieces of parallel data signals (k: 2 or larger natural number), output terminals for outputting "j" pieces of parallel data signals and "j" pieces of parallel clock input terminals, decides and recovers "j x k" pieces of data signals which are input to the input terminals and the data rate of each of which is f1/k b/s using "j" pieces of multiplied clock signals applied to "j" pieces of parallel clock input terminals via "j+1"th to "2 x j "th interconnects as a criterion of timing, performs time-division multiplexing in the ratio of "k1" and converts to "j " pieces of data signals the data rate of each of which is f1 b/s, wherein:

the terminals for receiving "j x k" pieces of parallel data signals of the synchronous digital circuit function as the input terminals of the transmitter circuit and the terminals for outputting "j" pieces of parallel data output signals function as the output terminals of the transmitter circuit; and

first to "j"th interconnects connecting the output terminal of the synchronous circuit and the input terminals of "j" pieces of multipliers and "j+1"th to "2 x j"th interconnects connecting the "j" pieces of multipliers and "j" pieces of parallel clock input terminals of the digital circuit are arranged so that delays t2max are smaller out of the maximum value t1max s of delays caused on the first to the "j"th interconnects and the maximum value t2max s of delays caused on the "j+1"th to the "2 x j"th

interconnects and the delays t2max are equivalent to 1/10 or less of a clock cycle 1/f1 s output from each multiplier.

Claim 19 is allowable because the prior art of record US Pub. No. 2004/0228636 to Pathak et al does not disclose to suggest a transceiver circuit comprising a receiver circuit and a transmitter circuit, wherein:

the receiver circuit comprises: a synchronous circuit that recovers and outputs a clock signal having a frequency of f1/n Hz (n: 2 or larger natural number) synchronized with input one data signal the data rate of which is f1 b/s (f1: positive real number) "j" pieces of multipliers that output each clock signal acquired by multiplying a clock signal output from the synchronous circuit by predetermined multiple ratio via "j" pieces of interconnects (j: one or larger natural number); and

a synchronous digital circuit that has "j" pieces of parallel input terminals including one common to the input of the synchronous circuit, "j x k" pieces of parallel output terminals and "j" pieces of parallel clock input terminals, decides and recovers "j" pieces of data signals the data rate of each of which is f1 b/s and which are input to the "j" pieces of parallel input terminals using the "j" pieces of multiplied clock signals applied to the "j " pieces of parallel clock input terminals via (j+1) th to (2 x j) th interconnects as a criterion of timing, demultiplexes the data in the ratio of "1:k" and converts to "j x k" pieces of data signals the data rate of each of which is f1/k b/s, wherein:

the "j" pieces of parallel terminals to which data signals are input of the synchronous digital circuit function as the input terminal of the receiver circuit and the "j x k" pieces of parallel terminals from which the data signals are output function as the output terminal of the receiver circuit; and

first to "j"th interconnects connecting the output terminal of the synchronous circuit and the input terminals of the "j" pieces of multipliers and "j+1"th to "2 x j"th interconnects connecting the "j" pieces of multipliers and the "j" pieces of parallel clock input terminals of the digital circuit are arranged so that delays t2max are smaller out of the maximum value t1max s of delays caused on the first to the "j"th interconnects and the maximum value t2max s of delays caused on the "j+1"th to the "2 x j"th interconnects and the delays t2max are equivalent to 1/10 or less of a clock cycle 1/f1 s output from each multiplier, wherein:

the transmitter circuit comprises:

a synchronous circuit to which a clock signal having a frequency of f1/m/n Hz (f1: positive real number, m: one or larger natural number, n: 2 or larger natural number) is input and from which a clock signal having a frequency of f1/n Hz and synchronized with the input clock signal is output;

"j" pieces of multipliers to which the clock signals output from the synchronous circuit are input via first to "j "th (j: one or larger natural number) interconnects and from each of which a clock signal multiplied by predetermined multiple ratio is output; and

a synchronous digital circuit that has input terminals for receiving "j x k" pieces of parallel data signals (k: 2 or larger natural number), output terminals for outputting "j" pieces of parallel data signals and pieces of parallel clock input terminals, decides and recovers "j x k" pieces of data signals which are input to the input terminals and the data rate of each of which is f1/k b/s using "j" pieces of multiplied clock signals applied to "j" pieces of parallel clock input terminals via "j+1"th to "2 x j" th interconnects as a criterion of timing, performs time-division multiplexing in the ratio of "k:1" and converts to "j" pieces of data signals the data rate of each of which is f1 b/s, wherein:

the terminals for receiving "j x k" pieces of parallel data signals of the synchronous digital circuit function as the input terminals of the transmitter circuit and the terminals for outputting "j" pieces of parallel data output signals function as the output terminals of the transmitter circuit; and

first to "j"th interconnects connecting the output terminal of the synchronous circuit and the input terminals of "j" pieces of multipliers and "j+1"th to "2 x j"th interconnects connecting the "j" pieces of multipliers and "j" pieces of parallel clock input terminals of the digital circuit are arranged so that delays t2max are smaller out of the maximum value t1max s of delays caused on the first to the "j"th interconnects and the maximum value t2max s of delays caused on the "j+1"th to the "2 x j"th interconnects and the delays t2max are equivalent to 1/10 or less of a clock cycle 1/f1 s output from each multiplier.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Trinh et al (US Patent No. 6,999,543) is cited to show clock data recovery deserializer with programmable sync detect logic.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalzid Singh whose telephone number is (571) 272-3029. The examiner can normally be reached on Mon-Fri 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DS
November 24, 2006
David Singh